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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/645,880	08/25/2000	Megumi Yokoi	1614.1069	4079
21171	7590	05/21/2004	EXAMINER	
STAAS & HALSEY LLP SUITE 700 1201 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			TRAN, DENISE	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/645,880	YOKOI ET AL.
	Examiner	Art Unit
	Denise Tran	2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 16 March 2004.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-17 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 25 August 2000 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5) Notice of Informal Patent Application (PTO-152)
6) Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/27/04 has been entered.

2. The applicant's amendment filed 3/17/03 has been considered. Claims 1-17 are presented for examination. Claims 18-34 have been canceled.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carpenter et al., U.S. Patent No. 6,067,611, hereinafter Carpenter in view of Irie et al., U.S. Patent No. 6,263,405, hereinafter Irie.

As per claim 1, Carpenter shows the use of a memory access method for a multiprocessor system (e.g. fig. 1) which includes a plurality of system modules (e.g. fig.

1, elements 10a-10d) coupled via a crossbar module (e.g. fig. 1, element 22 and col. 4, line 65 to col. 5, line 1), each of the system modules including a buffer (e.g. fig. 2C, element 52, col. 2, lines 46-60 and col. 11, lines 4-24) which holds the data and a plurality of processors (e.g. fig. 1, CPUs) having a cache memory (e.g. fig. 1, elements L2 and col. 3, lines 40-45) which temporarily holds data, said memory access method comprising:

responsive to a read request from a processor within an arbitrary system module, holding data from one of the system modules, other than the arbitrary system module (e.g. col. 2, lines 40-60).

Carpenter does not specifically show the use of a preread and a buffer within the crossbar to hold the data preread from one of the system modules, other than the arbitrary system module and wherein the data preread is data at a location that is close to the processor that made the read request. Irie shows the use of a preread and a buffer within the crossbar to hold the data preread from a system module, other than the arbitrary system module (e.g. fig. 9, parallel branches starting at steps 905 and 908 before judging based on the coherency status summary; col. 6, line 49 to col. 7, line 12 and col. 7, lines 44-50; fig. 1, element 40; fig. 6, element 400-2 and col. 10, lines 4-5) and wherein the data preread is data at a location that is close to the processor that made the read request (e.g. figure 1, PROCESSOR BOARD 1 is close to PROCESSOR BOARD 2 and col. 7, lines 20-40). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Irie into Carpenter's

system because it would provide for a reduction in memory latency when a cache miss occurs and allow the data to be in closer proximity to the requesting processor.

As per claim 5, Carpenter shows the use of a multiprocessor system, comprising:
a plurality of system modules (e.g. fig. 1, elements 10a-10d);
at least one crossbar module (e.g. fig. 1, element 22 and col. 4, lines 65 to col. 5, line 1); and

a bus coupling the system modules and crossbar module (e.g. fig. 2A, elements 28 and 32 and fig. 2C, elements "TO NODE INTERCONNECT ADDRESS PATH" and "TO NODE INTERCONNECT DATA PATH");

each of the system modules including a buffer which holds data (e.g. fig. 2C, element 52, col. 2, lines 46-60 and col. 11, lines 4-24), a plurality of processors (e.g. figure 1, CPUs) each having a cache memory which temporarily holds the data (e.g. fig. 1, elements L2 and col. 3, lines 40-45), and a control unit which controls input and output of the data with respect to the system module to which the control unit belongs (e.g. fig. 1, element 20 and fig. 2C);

a data transfer between two of the system modules being made via the crossbar module (e.g. fig. 1, element 22, and col. 5, lines 52-67); and

said crossbar module responsive to a read request from a processor within an arbitrary system module (e.g. abstract and col. 4, lines 65 to col. 5, line 1).

Carpenter does not specifically show the use of a preread and a buffer within the crossbar to hold the data preread from one of the system modules, other than the

arbitrary system module and wherein the data preread is data at a location that is close to the processor that made the read request. Irie shows the use of a preread and a buffer within the crossbar to hold the data preread from a system module, other than the arbitrary system module (e.g. fig. 9, parallel branches starting at steps 905 and 908 before judging based on the coherency status summary; col. 6, line 49 to col. 7, line 12 and col. 7, lines 44-50; fig. 1, element 40; fig. 6, element 400-2 and col. 10, lines 4-5) and wherein the data preread is data at a location that is close to the processor that made the read request (e.g. figure 1, PROCESSOR BOARD 1 is close to PROCESSOR BOARD 2 and col. 7, lines 20-40). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Irie into the system's Carpenter because it would provide for a reduction in memory latency when a cache miss occurs and allow the data to be in closer proximity to the requesting processor.

5. Claims 2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carpenter et al., U.S. Patent No. 6,067,611, hereinafter Carpenter, in view of Irie et al., U.S. Patent No. 6,263,405, hereinafter Irie, as applied to claims 1 and 5 above, and in further view of Christie, U.S. Patent No. 6,055,650.

As per claims 2, 6, Carpenter and Irie do not specifically show the use of (unit) setting information indicating whether or not to carry out a data preread with respect to the arbitrary system module, depending on a program which is executed by one or a plurality of processors within the arbitrary system module. Christie shows the use of (unit) setting information indicating whether or not to carry out a data preread with

respect to the arbitrary system module, depending on a program which is executed by one or a plurality of processors within the arbitrary system module (e.g. col. 2, lines 36-68 and col. 5, line 51 to col. 6, line 35). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Christie with the combined system of Carpenter and Irie because it would provide for an increase in performance by disabling accessing which are incorrect and reduce memory bandwidth conflicts, as taught by Christie, col. 2, lines 21-34.

6. Claims 4, 8, and 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carpenter et al., U.S. Patent No. 6,067,611, hereinafter Carpenter in view of Irie et al., U.S. Patent No. 6,263,405, hereinafter Irie, as applied to claims 1 and 5 above, and in further view of Hooks et al., U.S. Patent No., 5,761,452, hereinafter Hooks.

As per claims 4 and 8, Carpenter and Irie do not specifically show the use of (unit) adding, to a data transfer of the preread data, a priority which is lower than a priority of a normal data transfer. Hooks shows the use of (unit) adding, to a data transfer of the preread data (i.e., speculative pre-fetch), a priority which is lower than a priority of a normal data transfer (e.g. col. 5, lines 17-25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Hooks into the combined system of Carpenter and Irie because it would provide for the prevention of more important transactions from not being performed. Sometimes the preread will not be necessary if the data is in one of the caches. Therefore, it is

obvious that a transaction that needs to be performed is more important than a transaction that might be performed as taught by Hooks, col. 1, lines 53-62.

As per claims 12, 14, Carpenter does not specifically show the use of generating the read request from the arbitrary system module if a mishit occurs in the arbitrary system module, prereading the data requested by the read request in the system module, other than the arbitrary system module, and storing the requested data, and transferring the preread data from the system module, other than the arbitrary system module, to the buffer within the crossbar module, with a priority lower than a priority of a normal data transfer between the system modules and the crossbar module. Irie shows the use of generating the read request from the arbitrary system module if a mishit occurs in the arbitrary system module (e.g. col. 6, lines 51-54 or col. 7, lines 21-25), prereading the data requested by the read request in the system module, other than the arbitrary system module, and storing the requested data, and transferring the preread data from the system module, other than the arbitrary system module, to the buffer within the crossbar module (e.g. col. 6, line 54 to col. 7, line 12 or col. 7, lines 25-35 and col. 10, lines 3-5). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Irie into the system's Carpenter because it would provide for a reduction in memory latency when a cache miss occurs and allow the data to be in closer proximity to the requesting processor. Hooks shows the use of adding, to a data transfer of the preread data (i.e., speculative pre-fetch), a priority which is lower than a priority of a normal data transfer (e.g. col. 5, lines 17-25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Hooks into the combined system of Carpenter and Irie because it would provide for the prevention of more important transactions from not being performed. Sometimes the preread will not be necessary if the data is in one of the caches. Therefore, it is obvious that a transaction that needs to be performed is more important than a transaction that might be performed as taught by Hooks, col. 1, lines 53-62.

As per claims 13, 15, Carpenter does not specifically show the use of transferring the preread data stored in the buffer within the crossbar module to the arbitrary system module. Irie shows the use of transferring the preread data stored in the buffer within the crossbar module to the arbitrary system module (e.g. col. 7, lines 6-8 or 35-37). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Irie into the system's Carpenter because it would provide for a reduction in memory latency when a cache miss occurs and allow the data to be in closer proximity to the requesting processor to be received. Furthermore, Carpenter and Irie do not specifically show the use of adding, to a data transfer of the preread data, a priority which is lower than a priority of a normal data transfer. Hooks shows the use of adding, to a data transfer of the preread data (i.e., speculative pre-fetch), a priority which is lower than a priority of a normal data transfer (e.g. col. 5, lines 17-25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Hooks into the combined system of Carpenter and

Irie because it would provide for the prevention of more important transactions from not being performed. Sometimes the preread will not be necessary if the data is in one of the caches. Therefore, it is obvious that a transaction that needs to be performed is more important than a transaction that might be performed as taught by Hooks, col. 1, lines 53-62.

7. Claims 3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carpenter et al., U.S. Patent No. 6,067,611, hereinafter Carpenter in view of Irie et al., U.S. Patent No. 6,263,405, hereinafter Irie, as applied to claims 1 and 5 above, in further view of Christie, U.S. Patent No. 6,055,650 and in further view of Hooks et al., U.S. Patent No., 5,761,452, hereinafter Hooks.

As per claims 3, 7, Carpenter, Irie and Christie do not specifically show the use of (unit) adding, to a data transfer of the preread data, a priority which is lower than a priority of a normal data transfer. Hooks shows the use of (unit) adding, to a data transfer of the preread data (i.e., speculative pre-fetch), a priority which is lower than a priority of a normal data transfer (e.g. col. 5, lines 17-25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Hooks into the combined system of Carpenter, Irie and Christie because it would provide for the prevention of more important transactions from not being performed. Sometimes the preread will not be necessary if the data is in one of the caches. Therefore, it is obvious that a transaction that needs to be performed is more important than a transaction that might be performed as taught by Hooks, col. 1, lines 53-62.

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Carpenter et al., U.S. Patent No. 6,067,611, hereinafter Carpenter in view of Irie et al., U.S. Patent No. 6,263,405, hereinafter Irie , as applied to claim 5 above, and in further view of Pong, U.S. Patent No. 6,341,337.

As per claim 9, Carpenter and Irie do not specifically show the use of wherein one of the system modules, which has a memory with a requested address of the read request, includes unit starting a data preread at a timing before detecting a state of the cache memory included therein. Pong shows the use of wherein one of the system modules, which has a memory with a requested address of the read request, includes a unit starting a data preread at a timing before detecting a state of the cache memory included therein (e.g. fig. 6, branch of elements starting with 302 and 312 and col. 7, lines 25-60). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Pong into the combined system of Carpenter and Irie because it would provide for the distributed control of the preread and a reduction in bus traffic as taught by Pong col. 4, lines 9-11.

9. Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carpenter et al., U.S. Patent No. 6,067,611, hereinafter Carpenter in view of Irie et al., U.S. Patent No. 6,263,405, hereinafter Irie and in further view of Venkitakrishnan, U.S. Patent No. 6,263,415.

As per claims 10, 11, Carpenter shows the use of a multiprocessor system comprising:

a plurality of nodes (e.g. figure 1, elements 10a-10d) each including a system module (e.g. figure 1, elements 10a-10d), a bus coupling the system modules and the crossbar module (e.g. figure 2A, elements 28 and 32 and figure 2C, elements "TO NODE INTERCONNECT ADDRESS PATH" and "TO NODE INTERCONNECT DATA PATH"); and

each of the system modules including a buffer which holds data (e.g. figure 2C, element 52, col. 2, lines 46-60 and col. 11, lines 4-24), a plurality of processors (e.g. fig. 1, CPUs) each having a cache memory which temporarily holds the data (e.g. figure 1, elements L2 and col. 3, lines 40-45) and a control unit which controls input and output of the data with respect to the system module to which the control unit belongs (e.g. figure 1, element 20 and figure 2C),

a data transfer between two of the system modules being made via at least one crossbar module (e.g. figure 1, element 22, and col. 5, lines 52-67), and

said crossbar module responsive to a read request from a processor within an arbitrary system module (e.g. abstract and col. 4, lines 65 to col. 5, line 1).

Carpenter does not specifically show the use of the node having a plurality of system modules and a crossbar, a bus coupling adjacent nodes via the crossbar modules of the adjacent node, a preread and a buffer within the crossbar to hold the data preread from one of the system modules, other than the arbitrary system module and wherein the data preread is data at a location that is close to the processor that

made the read request. Irie shows the use of a preread and a buffer within the crossbar to hold the data preread from a system module, other than the arbitrary system module (e.g. fig. 9, parallel branches starting at steps 905 and 908 before judging based on the coherency status summary; col. 6, line 49 to col. 7, line 12 and col. 7, lines 44-50; fig. 1, element 40; fig. 6, element 400-2 and col. 10, lines 4-5) and wherein the data preread is data at a location that is close to the processor that made the read request (e.g. figure 1, PROCESSOR BOARD 1 is close to PROCESSOR BOARD 2 and col. 7, lines 20-40). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Irie into the system's Carpenter because it would provide for a reduction in memory latency when a cache miss occurs and allow the data to be in closer proximity to the requesting processor.

Venkitakrishnan shows the use of the node having a plurality of system modules (e.g. fig. 1, elements 200+300 and 400+500) and a crossbar (e.g. fig. 1, element 600 and 700), a bus coupling adjacent nodes via the crossbar modules of the adjacent node (e.g. fig. 1, connections between XBS). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Venkitakrishnan into the combined system of Carpenter and Irie because it would provide for a reduction of signal lines between crossbars (i.e., sharing a crossbar between two system modules) and provide for the ease of expandability of the system (i.e., adding nodes without having to replace the central crossbar switch).

10. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carpenter et al., U.S. Patent No. 6,067,611, hereinafter Carpenter in view of Irie et al., U.S. Patent No. 6,263,405, hereinafter Irie and in further view of Venkitakrishnan, U.S. Patent No. 6,263,415 and Hooks et al., U.S. Patent No., 5,761,452, hereinafter Hooks.

As per claim 16, Carpenter does not specifically show the use of generating the read request from the arbitrary system module if a mishit occurs in the arbitrary system module, prereading the data requested by the read request in the system module, other than the arbitrary system module, and storing the requested data, and transferring the preread data from the system module, other than the arbitrary system module, to the buffer within the crossbar module, with a priority lower than a priority of a normal data transfer between the system modules and the crossbar module. Irie shows the use of generating the read request from the arbitrary system module if a mishit occurs in the arbitrary system module (e.g. col. 6, lines 51-54 or col. 7, lines 21-25), prereading the data requested by the read request in the system module, other than the arbitrary system module, and storing the requested data, and transferring the preread data from the system module, other than the arbitrary system module, to the buffer within the crossbar module (e.g. col. 6, line 54 to col. 7, line 12 or col. 7, lines 25-35 and col. 10, lines 3-5). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Irie into the system's Carpenter because it would provide for a reduction in memory latency when a cache miss occurs and allow the data to be in closer proximity to the requesting processor. Hooks shows the use of

adding, to a data transfer of the preread data (i.e., speculative pre-fetch), a priority which is lower than a priority of a normal data transfer (e.g. col. 5, lines 17-25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Hooks into the combined system of Carpenter and Irie because it would provide for the prevention of more important transactions from not being performed. Sometimes the preread will not be necessary if the data is in one of the caches. Therefore, it is obvious that a transaction that needs to be performed is more important than a transaction that might be performed as taught by Hooks, col. 1, lines 53-62.

As per claim 17, Carpenter does not specifically show the use of transferring the preread data stored in the buffer within the crossbar module to the arbitrary system module. Irie shows the use of transferring the preread data stored in the buffer within the crossbar module to the arbitrary system module (e.g. col. 7, lines 6-8 or 35-37). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Irie into the system's Carpenter because it would provide for a reduction in memory latency when a cache miss occurs and allow the data to be in closer proximity to the requesting processor to be received. Furthermore, Carpenter and Irie do not specifically show the use of adding, to a data transfer of the preread data, a priority which is lower than a priority of a normal data transfer. Hooks shows the use of adding, to a data transfer of the preread data (i.e., speculative pre-fetch), a priority which is lower than a priority of a normal data transfer (e.g. col. 5, lines 17-25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Hooks into the combined system of Carpenter and Irie because it would provide for the prevention of more important transactions from not being performed. Sometimes the preread will not be necessary if the data is in one of the caches. Therefore, it is obvious that a transaction that needs to be performed is more important than a transaction that might be performed as taught by Hooks, col. 1, lines 53-62.

11. Applicant's arguments filed 3/16/04 have been considered but are not persuasive.

12. In the remarks, Applicants argued in substance that (1) the examiner's interpretation of the phrase "preread" is incorrect.

As to point (1) the examiner disagrees because as stated in the previous office action the examiner's interpretation is taken from Applicant's specification, page 1, lines 21-28. Applicant asserts the examiner is incorrect without specifying locations in the specification to show support of why the examiner is incorrect. Applicant is advised to please indicate where in the specification the definition of "preread" is different from the examiner's interpretation and Applicant's own specification page 1, lines 21-28.

13. In the remarks, Applicants argued in substance that (2) Irie does not teach or even suggest "holding data preread from one of the system modules, other than the

arbitrary system module, in a buffer with the crossbar module, wherein the data preread is data at a location that is close to the processor that made the read request" as recited in claim 1.

As to point (2) the examiner respectfully disagrees because Irie shows the use of a preread and a buffer within the crossbar to hold the data preread from a system module, other than the arbitrary system module (e.g. fig. 9, parallel branches starting at steps 905 and 908 before judging based on the coherency status summary; col. 6, line 49 to col. 7, line 12 and col. 7, lines 44-50; fig. 1, element 40; fig. 6, element 400-2 and col. 10, lines 4-5) and wherein the data preread is data at a location that is close to the processor that made the read request (e.g. figure 1, PROCESSOR BOARD 1 is close to PROCESSOR BOARD 2 and col. 7, lines 20-40).

14. In the remarks, Applicants argued in substance that (3) it is not obvious, even to those skilled in the art, to carry out the queuing/priority assignment of the memory preread within the crossbar module.

As to point (3) the examiner assumes Applicant is referring to claims 3-4, 7-8, 12, 14-17. However the examiner respectfully disagrees because Hooks shows the use of (unit) adding, to a data transfer of the preread data (i.e., speculative pre-fetch), a priority which is lower than a priority of a normal data transfer (e.g. col. 5, lines 17-25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Hooks into the combined system of Carpenter and Irie because it would provide for the prevention of more important transactions from not being

performed. Sometimes the preread will not be necessary if the data is in one of the caches. Therefore, it is obvious that a transaction that needs to be performed is more important than a transaction that might be performed as taught by Hooks, col. 1, lines 53-62.

15. In the remarks, Applicant argued in substance that (4) Irie does teach or suggest a buffer.

As to point (4) the examiner respectfully disagrees because Irie shows a buffer (e.g. fig. 6, element 400-2 and col. 10, lines 4-5). A queue is a buffer.

16. In the remarks, Applicant argued in substance that (5) Christie, Hooks, Pong and Venkitakrishnan do not teach or even suggest “responsive to a read request from a processor within an arbitrary system module, holding data preread from one of the system modules, other than the arbitrary system module, in a buffer with the crossbar module, wherein the data preread is data at a location that is close to the processor that made the read request” as recited in claim 1.

As to point (5) in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Christie, Hooks, Pong and Venkitakrishnan were not relied upon to show the above limitations, Irie was. Irie shows the use of a preread and a

buffer within the crossbar to hold the data preread from a system module, other than the arbitrary system module (e.g. fig. 9, parallel branches starting at steps 905 and 908 before judging based on the coherency status summary; col. 6, line 49 to col. 7, line 12 and col. 7, lines 44-50; fig. 1, element 40; fig. 6, element 400-2 and col. 10, lines 4-5) and wherein the data preread is data at a location that is close to the processor that made the read request (e.g. figure 1, PROCESSOR BOARD 1 is close to PROCESSOR BOARD 2 and col. 7, lines 20-40).

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (703) 305-9823. The examiner can normally be reached on Monday, Thursday and an alternated Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for central Official communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Denise Tran
D.T.
May 16, 2004